INSTRUCTION MEMORY HIERARCHY FOR AN EMBEDDED PROCESSOR

ABSTRACT OF THE DISCLOSURE

[0051] The present invention provides a processor with an instruction memory hierarchy and a method for distributing instructions to an array of multithreaded processing units organized in processor clusters. The instruction memory hierarchy comprises a processor cluster, an instruction request bus, an instruction request arbiter, and an instruction memory. The instruction request arbiter controls submissions of instruction requests from multithreaded processing units within the processor clusters to the instruction memory. The processor clusters send instruction requests responsive to a cache miss by a processor, or processor thread, within the processor cluster. The instruction request arbiter resolves conflicts between instruction requests attempting to access to a common cache set within the instruction memory. The instruction memory broadcasts instruction data to the processor clusters responsive to non-conflicting instruction requests forwarded from the instruction request arbiter.